REMARKS/ARGUMENTS

The specification has been amended to supply serial number and filing date information regarding an application referred to in the specification. No new matter has been added by the amendment.

Claims 1-9 and 13-24 are pending in the present application. Claims 1, 2, 13, 14, 22 and 23 were amended; and claims 10-12 have been canceled to expedite prosecution. No claims have been added. Support for the amendments to the claims can be found, for example, in Figure 17 and on page 46, line 4 to page 47, line 5. Applicants believe claims 1-9 and 13-24 patentably distinguish over the cited art and are allowable in their present form, and reconsideration of the rejection is respectfully requested in view of the above amendments and the following comments.

I. Double Patenting

Claims 1-8, 10-20 and 22-24 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-3, 6-8, 10-14, 16-19 and 22-28 of U.S. Application No. 10/806,094.

In order to expedite prosecution of the present application, a Terminal Disclaimer in compliance with 37 CFR 1.321(c) is enclosed herewith. Therefore, the rejection based on the judicially created doctrine of obviousness-type double patenting has been overcome.

II. Information Disclosure Statement

The Examiner advises that application 10/757,192 (labeled CE on page 3 of the Information Disclosure Statement submitted on June 30, 2005 was not considered because it is a duplicate application number of the application labeled CD).

The correct document is US Published Application 2005/0210454 A1 published 03-18-2004 of DeWitt, Jr. et al. A Supplemental Information Disclosure Statement is being filed concurrently herewith to disclose this document. Applicants regret this inadvertent error and appreciate the Examiner bringing it to their attention.

The Examiner also advises that articles labeled BJ and BM on page 2 of the Information Disclosure Statement filed June 30, 2005, have not been considered because they are not in English. It is noted, however, that English language abstracts were included with the documents, and it is respectfully requested that the Examiner acknowledge that he has considered the abstracts.

III. 35 U.S.C. § 102, Anticipation

The Examiner has rejected claims 1-3, 5-15, and 17-24 under 35 U.S.C. § 102(b) as being anticipated by Hervin et al. (U.S. Patent No. 5,805,879). This rejection is respectfully traversed.

In rejecting the claims, the Examiner states:

> With respect to claim 1, Hervin discloses a method in a data processing system for generating coverage data for accesses to data during execution of code in the data processing system, the method comprising:
>
> responsive to executing an instruction in the code at a processor in the data processing system, determining whether an access to a memory location associated with a data access indicator has occurred; and [(processor determines if the access indicator is to be set) column 3, lines 37-39]
>
> changing a state of the access indicator by the processor when the instruction is executed, the data access indicator is associated with the memory location, wherein coverage data is generated during execution of the code by the processor. [(whenever a memory is first accessed, set the access indicator associated therewith) column 3, lines 27-29]

Office Action dated May 4, 2006, pages 4-5.

Claim 1, as amended herein, is as follows:

> 1. A method in a data processing system for generating coverage data for accesses to data during execution of code in the data processing system, the method comprising:
>
> detecting that access to data in a memory location having a data access indicator associated therewith has occurred during execution of an instruction in the code at a processor in the data processing system; and
>
> changing a state of the data access indicator by the processor when the instruction is executed for generating coverage data for accesses to data during execution of the code by the processor.

A prior art reference anticipates a claimed invention under 35 U.S.C. § 102 only if every element of the claimed invention is identically shown in that single prior art reference, arranged as they are in the claims. *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). All limitations of a claimed invention must be considered when determining patentability. *In re Lowry*, 32 F.3d 1579, 1582, 32 U.S.P.Q.2d 1031, 1034 (Fed. Cir. 1994). Anticipation focuses on whether a claim reads on the product or process a prior art reference discloses, not on what the reference broadly teaches. *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 218 U.S.P.Q. 781 (Fed. Cir. 1983).

Applicants respectfully submit that Hervin et al. (hereinafter "Hervin") does not identically show every element of the claimed invention arranged as they are in the claims; and, accordingly, does not anticipate the claims. With respect to claim 1, in particular, Hervin does not teach or suggest "detecting that access to data in a memory location having a data access indicator associated therewith has occurred during execution of an instruction in the code at a processor in the data processing system"; or "changing

a state of the data access indicator by the processor when the instruction is executed for generating coverage data for accesses to data during execution of the code by the processor".

Hervin relates to setting a segment access indicator associated with a segment of system memory being accessed by a processor (see Abstract in Hervin). The mechanisms described in Hervin, however, operate differently than in the present invention as recited in amended claim 1. Specifically, the Examiner refers to col. 3, lines 27-29 and 37-39 of Hervin in rejecting the claims. Col. 3, lines 22-43 reads as follows:

> According to prior art x86-based architectures, typical execution of an instruction may initiate control sequences to facilitate certain operations in ones of the processing stages of the pipeline. One such operation sets a segment access indicator within the segment descriptor. More generally, whenever a segment in memory is first accessed, it has been conventional to set the segment access indicator associated therewith in one of the early processing stages. Setting of segment access indicators allows the identification of recently-accessed segments. This information is useful for a number of reasons, some of which are discussed in greater detail hereinbelow.
>
> In more recent x86-based processors, however, segment registers and segment descriptors are loaded late in the pipeline, typically in the execution processing stage, to increase the processor's throughput. By the time status checking circuitry within the processor determines that the segment access indicator is required to be set, the execution processing stage has already relinquished control of the earlier instruction decode and address calculation processing stages that are typically employed to set the segment access indicator.

Thus, in the above recitation, Hervin describes a problem in existing systems in that segment descriptors containing segment access indicators are typically loaded during the execution processing stage. Accordingly, detection of an access to a memory segment, and determination that a segment access indication is to be set occurs after the execution processing stage has "already relinquished control of the earlier instruction decode and address calculation processing stages that are typically employed to set the segment access indicator".

In the present invention as recited in amended claim 1, on the other hand, it is detected "that access to data in a memory location having a data access indicator associated therewith has occurred during execution of an instruction in the code at a processor in the data processing system", and that a state of the data access indicator is changed by the processor "when the instruction is executed for generating coverage data for accesses to data during execution of the code by the processor". In other words, in Hervin, the segment access indicator is loaded during execution but is changed as a result of and following execution of an instruction. In the present invention, a state of the data access indicator is changed when the instruction is executed, as a result of detecting that access to data in a memory location

having a data access indicator associated therewith has occurred. Hervin does not disclose detecting access to a memory location and changing a state of a data access indicator during execution of code as recited in claim 1, and, accordingly, does not anticipate claim 1. Claim 1, accordingly, patentably distinguishes over Hervin in its present form, and it is respectfully requested that the Examiner so find.

Claims 2, 3 and 5-9 depend from and further restrict claim 1, and are also not anticipated by Hervin, at least by virtue of their dependency. In addition, these claims recite additional subject matter not disclosed or suggested by Hervin. For example, claim 2, as amended herein recites:

> 2. The method of claim 1, wherein the changing step comprises:
> receiving a signal at a data cache in the processor generated by a completion buffer in the processor indicating that data in the memory location has been accessed during the execution of the instruction; and
> responsive to receiving the signal, changing the state of the access indicator by the data cache.

The Examiner refers to col. 4, lines 24-43, reproduced below as disclosing this feature.

> In one embodiment of the present invention, the circuit further comprises status checking circuitry that examines a segment descriptor containing the segment access indicator for a status of bits in the segment descriptor. The status checking circuitry generates the exception when the segment access indicator is in a zero state. As will be described more particularly, the process of gaining access to a different segment begins with a segment descriptor pertaining to the different segment being loaded into special registers within the processor. After the segment descriptor is retrieved from memory, the status checking circuitry examines status bits within the segment descriptor, the status bits indicating various statuses with respect to the segment. The segment access indicator, one of the status bits, indicates whether the segment described by the segment descriptor has, or has not, been accessed. Operating systems that swap segments between volatile and nonvolatile memory use the segment access indicators of the segments to determine when accessed segments should be written to nonvolatile memory to preserve their contents.

The above recitation describes that status checking circuitry examines a segment descriptor containing a segment access indicator. Nowhere in the above recitation is it described that the state of the segment access descriptor is changed "in response to receiving a signal generated by a completion buffer in the processor indicating that data in the memory location has been accessed during the execution of the instruction" as recited in claim 2. Claim 2, accordingly, is not anticipated by Hervin in its own right as well as by virtue of its dependency.

Independent claims 13 and 22 have been amended in a manner similar to claim 1, and are also not anticipated by Hervin for similar reasons as discussed above with respect to claim 1. Claims 14-15, 17-21

and 23-24 depend from and further restrict one of claims 13 and 22 and are also not anticipated by Hervin, at least by virtue of their dependency and for reasons discussed above with respect to claim 2.

Therefore, the rejection of claims 1-3, 5-15, and 17-24 under 35 U.S.C. § 102 has been overcome.

IV. 35 U.S.C. § 103, Obviousness

The Examiner has rejected claims 4 and 16 under 35 U.S.C. § 103(a) as being unpatentable over Hervin et al. (U.S. Patent No. 5,805,879) in view of Sederlund et al. (U.S. Patent No. 6,647,301 B1). This rejection is respectfully traversed.

The Examiner cites Sederlund as disclosing a "memory access error indicator with shadow memory". Sederlund does not, however, supply the deficiencies in Hervin as described above, and claims 4 and 16 are allowable in their present form at least by virtue of their dependency.

Therefore, the rejection of claims 4 and 16 under 35 U.S.C. § 103 has been overcome.

V. Conclusion

For all the above reasons, it is respectfully urged that claims 1-9 and 13-24 are allowable in their present form, and that this application is now in condition for allowance. It is, accordingly, respectfully requested that the Examiner so find and issue a Notice of Allowance in due course.

The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

DATE: August 4, 2006

Respectfully submitted,

/Gerald H. Glanzman/

Gerald H. Glanzman
Reg. No. 25,035
Yee & Associates, P.C.
P.O. Box 802333
Dallas, TX 75380
(972) 385-8777
Attorney for Applicants